RESEARCH ARTICLE

Design of a MEMS-Based Oscillator Using 180nm CMOS Technology

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Abstract

Micro-electro mechanical system (MEMS) based oscillators are revolutionizing the timing industry as a cost effective solution, enhanced with more features, superior performance and better reliability. The design of a sustaining amplifier was triggered primarily to replenish MEMS resonator's high motion losses due to the possibility of their 'system-on-chip' integrated circuit solution. The design of a sustaining amplifier observing high gain and adequate phase shift for an electrostatic clamp-clamp (C-C) beam MEMS resonator, involves the use of an 180nm CMOS process with an unloaded Q of 1000 in realizing a fixed frequency oscillator. A net 122dBΩ transimpedance gain with adequate phase shift has ensured 17.22MHz resonant frequency oscillation with a layout area consumption of 0.121 mm² in the integrated chip solution, the sustaining amplifier draws 6.3mW with a respective phase noise of -84dBc/Hz at 1kHz offset is achieved within a noise floor of -103dBc/Hz. In this work, a comparison is drawn among similar design studies on the basis of a defined figure of merit (FOM). A low phase noise of 1kHz, high figure of merit and the smaller size of the chip has accredited to the design's applicability towards in the implementation of a clock generative integrated circuit. In addition to that, this complete silicon based MEMS oscillator in a monolithic solution has offered a cost effective solution for industrial or biomedical electronic applications.

Introduction

Reference frequency sources typically generate a single frequency ranging from 1MHz to 50MHz for the use of a channel rate and multi clock domain phase locked loops (PLL), which synthesizes an output ranging from lower megahertz to over 1GHz. Present electronic devices, such as personal computers, servers and embedded systems are in need of timing clocks to achieve synchronization of operation. However, frequency accuracy is flexed in some data interface protocols, such as HS-USB, S-ATA and 10/11/1000 Ethernet, where higher ppm is in need. For example, reference oscillator in USB 2000 maintains ±500ppm, serial ATA 2005 needs ±350 and IEEE Std. 1998 needs ±100ppm [1–3].

roles of these authors are articulated in the 'author contributions' section.

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In the past, bulky off-chip quartz based ICs were the preferred choice for reference timing generation. Comparatively, MEMS electrostatic resonator based oscillator proved its significance with its system-on-chip (SoC) solution where an inductorless design proved an excellent supplementary choice for the RC-VCO, complying with OC-48 application criteria [4, 5]. Nevertheless, the electrostatic resonator based oscillator lags with some setbacks in some dedicated applications, but exhibits promising performances in the application of real time clocking (RTC) with a comparatively low output signal level in the MEMS based oscillator, due to the high motional losses of the resonator. The RTC adaptation was deemed appropriate as low signal levels and jitter/noise pattern exhibits no major concern in the clocking application of [6–8]. Potential biomedical application of portable optical needle substitution by CMOS circuitry [9], is an example to be cited in this work, as the RTC employed chip technology can perform on par with the previously used bulky equipment, to offer logical functions needed for the optical resolution of tissue planes. At its strongest point, clock IC's are desirably miniaturized through the implementation of MEMS device, as its favorable small form factor edges over its quartz counterpart.

Two distinct resonator actuations for MEMS structures are piezoelectric and capacitive. The piezoelectric actuation naturally exhibits much lower motional resistance and a higher power handling capability than the actuation in electrostatic resonator [10, 11]. In the view of SoC implementation, onto low cost silicon substrate, capacitive-based electrostatic resonators leads in preference [12–14]. As such, the sustaining amplifier is loaded with the Q factor of the resonator in the oscillator. The capacitive-based resonator limits the operation bandwidth of the transimpedance amplifier (TIA), thus limiting the oscillation range. This work depicts the design and implementation of CMOS based single ended sustaining amplifier in sustaining the oscillation of a MEMS resonator. The objective of the work is to deliver a highly competitive performance oscillator through the optimization of phase noise and power dissipation in the application of clock generation IC. A comparatively low cost, temperature uncompensated Si clamp-clamp beam resonator is chosen for a much higher figure of merit realization of the complete electrostatic oscillator. For the oscillator, the operation frequency is 17.22MHz with a 95% yield of frequency in 180nm CMOS process implementation. Now, section 2 of this paper reports the descriptive characteristic of the MEMS resonator in MHz application, followed by the review on the design of the sustaining amplifier in Section 3. Section 4 summarizes the experimental and simulation results obtained. It also encapsulates a discussion by comparing the performance of the proposed work with other similar works and a process corner sustainability study of the post layout design through Monte Carlo simulation tools. Lastly, the conclusion of this work is given in Section 5.

Electrostatic MEMS Resonator

The operations of MEMS sensing can be realized as common base, resistive or capacitive detection [15]. The common base detection and resistive detection, exhibits higher noise effect compared to its counterpart, of capacitive detection. Common base detection has an input of current noise which is proportional to the increase of the transconductance of the input MOS, whereas in the resistive detection amplifier, noise is dominated by the conversion resistance, resulting in reduced bandwidth of operation [16]. Since noise seems to be the governing performance factor in the intended application of clock ICs, capacitive detection is deemed to be the least noisiest is avoided in appreciating the degrading parasitic effects resulting to the reduction in bandwidth [17, 18].

In MEMS devices, air damping, thermos-elastic damping and acoustic energy loss in anchors are contributing sources of mechanical loss. Although vacuum packaging is used to

suppress air damping in present C-C MEMS, the major contribution of loss is due to the periodic wave to the anchor.

Design of Sustaining Amplifier

In sustaining the oscillation, an integrating amplifier is essential with a positive gain and a sufficient phase shift [15]. In this work, a CMOS based single ended-single rail amplifier is integrated as the sustaining amplifier circuit. The circuit desirably inherits sufficient gain-bandwidth in the feedback compensation. The architecture is targeted to exhibit competitive phase noise, with minimal DC power dissipation, leading towards a promising Figure of Merit (FOM) with an acceptable output voltage swing.

In this work, the sustaining amplifier consists of a transimpedance amplifier (TIA), followed by a non-inverting voltage amplifier and subsequently a cascode stage. The amplifier is terminated with a 50Ω output buffer for characterization purposes. The ‘capacitively read’ motional current is fed into the TIA and reintroduced back to electrostatically excite the resonator. A topology based feedback analysis technique can be interpreted in deriving the gain and output resistances for each particular stage of this sustaining amplifier which gets support from [19], [20] and [21].

Design of transimpedance amplifier stage

The C-C beam resonator operates in electrostatic capacitive transduction mode, generates a small alternating current signal in its read-out electrode. In this work, a regulated cascode (RGC), shunt-shunt feedback TIA is developed, where the feedback resistor has been divided into two equal parts to ensure better linearity. Fig 1 shows the schematic of the TIA, which inherits high gain, high linearity and low noise performance. Fig 1 illustrates, the core of the amplifier consists of a common source stage and a source follower stage. The source follower isolates the resistor, R_3 from the loading effect of the feedback resistors R_2 and R_4 . The closed loop gain is made adjustable by R_2 and R_4 , in a pre-condition that the output impedance of the source follower is kept much lesser than the feedback resistor.

Fig 1. Transimpedance amplifier schematic diagram along with bias circuitry. a) Feedback resistor being divided into R_2 and R_4 for enhancing linearity b) Equivalent feedback resistor R_F c) The small signal equivalent model.

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When current from MEMS is zero, then the gate voltage of M_4 is equal to the DC value of output voltage, v_{out} . As i_{MEMS} increases, most of the current will flow through R_4 and sink via the current source. Along with this, the current flow through M_3 and R_2 will also be increased in which, the MEMS output current is converted and sensed as a voltage drop signal across R_2 . However, for a substantial increase in i_{MEMS} , the voltage drop across R_4 will reduce v_{out} and the current source is driven into the linear region of operation, hence sacrificing the linearity. R_4 is designed to have a minimum value in maintaining the linearity, whereas R_2 is adjusted for high gain/noise performance.

Fig 1 illustrates the working principle of the TIA. In reference to Fig 1(a), the output voltage, V_{out} is sensed and its proportional current is routed through R_2 back to the summing point, V_Y at its input. At this point, V_Y shunt-shunt feedback is actuated and simultaneously linearity is enhanced by dividing R_F into R_2 and R_4 . The gain expression developed in reference to Fig 1 (b), is given as in Eq (1).

$$V_{in} - V_{out} = I_{RF} \times R_F \quad (1)$$

Considering, $I_{bias} = (I_{MEMS} + I_{R2})$ and $I_{RF} = I_{MEMS} = I_{R4}$, the voltage V_x at the node of R_3 can be written as $V_x = -(g_{m3} \times R_3 \times V_{in}) = V_{out}$, from which the open loop gain is obtained.

$$\frac{V_{out}}{V_{in}} = -g_{m3} \times R_3 \quad (2)$$

Substituting Eq (2) into Eqs (1) and (3) can be yielded.

$$\frac{V_{out}}{I_{MEMS}} = \frac{-R_F(g_{m3}R_3)}{1 + g_{m3}R_3} \quad (3)$$

With the incorporation of R_2 and R_4 in increasing its stability, the output voltage is derived hereby.

$$\begin{aligned} V_{in} - V_{out} &= I_{MEMS} \times R_4 \times I_{R2} \times R_2 \\ \Rightarrow V_{out} \left(\frac{1}{-g_{m3}R_3} - 1 \right) &= I_{MEMS}(R_4 - R_2) + I_{R3}R_2 \\ \Rightarrow V_{out} &= I_{MEMS} \left(\frac{(-g_{m3}R_3)(R_4 - R_2)}{1 + g_{m3}R_3} \right) + I_{R3} \left(\frac{(-g_{m3}R_3)(R_2)}{1 + g_{m3}R_3} \right) \end{aligned} \quad (4)$$

By comparing Eq (3) with Eq (4), it is evident that, in the resistive feedback configuration, when I_{MEMS} or V_{in} is increased, the slope of Eq (4) decreases. With this increased linearity and better stability, the close loop transimpedance gain, R_T can be derived. In considering a larger aspect ratio of M_3 , it can be deduced that, $(1/g_{m3}) \ll (R_2 + R_4)$ for which the output impedance referring into the source follower (consists of M_3 and current source) approximates to $1/g_{m3}$. Thus, the close loop transimpedance gain, defined by R_T becomes the sum of the adjustable resistances in the feedback loop as seen in Eq (5), in the event that the open loop gain of Eq (2) is much greater than unity.

$$R_T = \frac{g_{m3}R_3}{1 + g_{m3}R_3} \times (R_4 + R_2) \approx (R_4 + R_2) \quad (5)$$

Design of an intermediate stage voltage amplifier

Subsequently, after the read-out signal is acquired as the capacitive current from the MEMS resonator and converted into a voltage signal by the TIA, the voltage amplifier follows with enhanced gain and extended bandwidth operation. There is a necessity of incorporating adequate phase shift from the input to output in sustaining the oscillation. In this work, a modified Cherry-Hooper voltage amplifier topology is designed for a nominal gain with zero phase shifts and an extended bandwidth. This block is designed to compensate the amount of gain, which is necessary to replenish the decrease of loop gain due to the relatively high load capacitance corresponding to the inputs of the integrating output buffers [22].

The schematic diagram of the voltage amplifier is shown in Fig 2. The push-pull inverter topology is chosen in preference for its simplicity and to enhance the output with less distortion per active device [23]. This second stage is the gain tuning stage achievable with the integration R_6 - C_2 "T" network. This "T" network in this shunt-shunt feedback configuration would introduce an extra zero, which will be used for pole cancellation in Eq (8) and offers less input and output impedance in subsequent stages of integration. As this R_6 - C_2 would favorably shift the poles to higher frequency, the bandwidth will also be increased. As observed from the small signal equivalent circuit, the expression of total gain could be derived for two back to back push pull amplifier circuits where the gain of each stage can be derived to be combined finally.

$$\frac{v_x}{v_{in}} = (g_{m5} + g_{m7})(r_{o5} || r_{o7}) \quad (6)$$

$$v_{R5} = (v_{out} - v_x) = (v_x) \left(\frac{sR_5 C_2}{1 + sR_5 C_2} \right) \quad (7)$$

Combining Eqs (6) and (7) while eliminating for v_x , the final voltage gain is obtained in Eq (8).

$$\frac{v_{out}}{v_{in}} = \frac{(g_{m5} + g_{m7})(r_{o5} || r_{o7})(1 + s2R_5 C_2)}{1 + sR_5 C_2} \quad (8)$$

From Fig 2(b), the output impedance can be written as shown in Eq (9).

$$z_{out} \approx \frac{(r_{o6} || r_{o8})R_6[R_5^2 + R_6(R_5 + r_{o5} || r_{o7})(R_5 C_2 s + 1)]}{(R_6 + r_{o6} || r_{o8})[R_5^2 + R_6(R_5 + r_{o5} || r_{o7})(R_5 C_2 s + 1)] + R_5(r_{o6} || r_{o8})[g_{m6}R_6(r_{o5} || r_{o7}) - R_5 + r_{o5} || r_{o7}]} \quad (9)$$

Capacitance, C_2 in Eq (9) will ensure a complete pole cancellation in extending the operational bandwidth. In this design, the transconductance of M_6 is kept much higher than the feedback resistance ($R_5 + R_6$) to avoid the phase shift resulting from the resistive loss. For a designated frequency ω_T in Eq (10), for which the pole would be cancelled, Eq (9) could be further simplified to acquire the desired output impedance given in Eq (11).

$$|\omega_T| \approx \frac{R_6 + R_5}{R_6 R_5 C_2} \quad (10)$$

$$\begin{aligned} z_{out} &\approx \frac{(r_{o6} || r_{o8})[(R_5 + R_6) + (r_{o5} || r_{o7})]}{(r_{o6} || r_{o8})[1 + g_{m6}(r_{o5} || r_{o7})]R_5 + (r_{o5} || r_{o7})} \\ \Rightarrow z_{out} &\approx \frac{(R_5 + R_6) + (r_{o5} || r_{o7})}{g_{m6}(r_{o5} || r_{o7})} \approx \frac{1}{g_{m6}} \end{aligned} \quad (11)$$

Fig 2. Intermediate voltage amplifier. a) Schematic diagram b) The small signal equivalent model.

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The value of R_5 and the aspect ratio of M_6 are tuned to replenish the gain, thus driving the targeted MEMS resonator. Also, as for its inverted buffer structure which consists of M_5 , M_6 , M_7 and M_8 , it ensures a near zero phase shift over the bandwidth of interest at 17.22 MHz of operation. This phase shift is necessary for sustaining the amplifier block, designed to comply the Barkhausen criterion.

Design of Cascode voltage amplifier stage

In the third stage of this single ended sustaining amplifier block, a cascode amplifier is integrated reflecting to additional voltage gain with a proportional phase shift. Cascode stage or the combination of common source (CS) and common gate (CG) amplifier is a good choice for high gain, with moderate input impedance and for an overall improved bandwidth operation. This configuration is deemed to be further stable as its output is electrically and physically isolated from the input.

In Fig 3, the CS amplifier is denoted with M_{10} , whereas M_{11} behaves as a CG stage. The feedback path from the output node to the gate of CS is through high resistance ($\sim 8k\Omega$), which is implemented by M_{15} and M_{16} , in a PMOS pseudo-resistor configuration. This feedback bias the CS stage (M_{10}), hence the output voltage signal from the previous stage of Fig 2, will assist this biasing through a 6pF decoupling capacitor, C_1 (not shown). Moreover, M_{12} gives an additional gain depending on the bias point of the CG stage. The current source consists of M_{13} , M_{14} and R_7 along with M_9 ensures the necessary biasing for CG stage. Fig 4(a), reflects a simplified representation of the cascode stage from which the small signal equivalent circuit is constructed in Fig 4(b). Referring to the nodes x and v_{out} , Eqs (12) and (13) can be derived.

$$(g_{o10} + g_{o11} + g_{m11}) \times v_x - g_{o11} \times v_{out} = -g_{m10} \times v_{in} \quad (12)$$

Fig 3. Cascode voltage amplifier with integrated bias circuitry consists of M₁, M₉, M₁₃, M₁₄, R₇ and R₁.

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$$(-g_{m11} - g_{o11}) \times v_x + (g_{o11} + g_{o12}) \times v_{out} = 0 \quad (13)$$

Solving Eqs (12) and (13), the desired gain expression is given as in Eq (14).

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m10}(g_{o11} + g_{m11})}{g_{o10}g_{o11} + g_{o10}g_{o12} + g_{o11}g_{o12} + g_{o12}g_{m11}} \cong \frac{-g_{m10}}{g_{o12}} \equiv -g_{m10} \times r_{o12} \quad (14)$$

Similarly, the output impedance can be found to be approximately equal to r_{o12} given by Eq (15).

$$r_{out} = [r_{o10} + r_{o11} + (g_{m11}r_{o10}r_{o11})] || (r_{o12}) \approx r_{o12} \quad (15)$$

Results and Discussion

In characterizing the design of the sustaining amplifier and further completing the oscillator architecture, several verification analyses have been done on a 0.18μm CMOS platform through the use of Cadence Spectre. Open loop responses are necessary to preliminarily determine the ability of the amplifier in compensating the motional losses which can be estimated from the resonator's forward transmission responses, S_{21} . Once the oscillation is configured to sustain via the Barkhausen criterion [3, 24, 25], then a close loop analysis for the whole resonator is discussed to measure the design's competence in a clock generator application with regards to frequency stability, phase noises, noise floor, etc.

MEMS characterization and parameters extraction

The referred C-C beam MEMS resonator is verified for its insertion loss and total phase shift estimation. In extracting the result, an experimental setup is constructed in extracting the scattering

Fig 4. Cascode voltage amplifier. a) Simplified schematic diagram with $8\text{ k}\Omega$ resistances b) The small signal equivalent model.

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parameter at the excited state of the resonator with an external DC bias of 5V. From this spectrum of data, the resonant frequency is observed at 17.22MHz. Other physical parameters, such as beam width, beam length, air gap, poisons co-efficient, and Young's modulus are used along with the resonant frequency to determine the electrical series RLC parameters constructing this resonator. The extracted RLC values in the lumped component model are verified from its spectrum analysis where it matches with the measured data, as described in Fig 5.

Fig 5. Resonator's behavioral response extracted by a spectrum analyzer. a) S_{21} magnitude plot b) S_{21} phase plot.

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In the model, the feed-through parasitic capacitance, C_p is approximated as 5.8fF by computing the capacitance from the overlap area between top and bottom electrodes. The edges are considered to be sharp enough for the overlap region and hence, the fringing field effect dominates. The value of C_p is found to be low from the geometry of the resonator and hence, it is assumed that parallel resonance does not force the resonator into non-linear vibration. The negligible deviation seen in the responses of Fig 5 are from unavoidable parasitic capacitances and resistances in real measurement apparatus, such as in the use of cable, ports, etc. The final component values for the two port electrical RLC model is shown in Fig 6 along with its simulated S-parameter analysis response. From this S_{21} response, an approximate 76dB of transmission loss can be found with a corresponding 95° phase shift. In Table 1, these findings are listed along with some main physical parameters of the MEMS device.

Sustaining amplifier open loop response

Each block of the amplifier delivers a prescribed amount of gain with a respective phase shift. In an open loop AC analysis, the individual responses are verified across the bandwidth of operation in the absence of the resonator, in completing the loop. In substitute of a resonator, a small AC current source with 17.22MHz is added as an input to emulate the role of capacitive current output of the MEMS resonator.

Fig 7 illustrates the responses from which a total open loop transimpedance gain is found at 122dBΩ with a phase shift of 70° at the operating frequency of 17.22MHz. Also, in Table 2, the corresponding gain and phase are summarized, contributing to this total transimpedance value.

To sustain the oscillation generated from the resonator model, the open loop gain must be above zero at the point of resonant frequency with the resonator included, confirming the Barkhausen criterion of oscillation [25]. The plot in Fig 8 illustrates the loop gain and phase shift at the operating frequency of 17.22MHz, which is observed to be 3.36dB and -1.12°, respectively.

Required TIA gain estimation. The insertion loss is estimated to be 76dB which is represented by motional R_x in Fig 6(a) for the C-C beam resonator, this loss ranges between several kΩ to a few MΩ and is dependent on the polarization voltage applied to it. While maintaining the linearity within the 90nm beam-electrode gap, for a bias of 5V, the reduced R_x is found to be 698kΩ in the present resonator. To sustain the oscillation in real time as quoted in F. Nabki's work in [25], the effective motional resistance should be at least 1.5 times of R_x , in dictating the minimum TIA gain. In this work, effective motional resistance is estimated to be $R_{motional} \geq 1.047M\Omega$. So, the minimum transimpedance gain that is adequate for sustaining the oscillation can be calculated as $20 \log(1.047M) \approx 120.398 \text{ dB}\Omega$. With respect to that, the referred value of the transimpedance gain is 122dBΩ given in Table 2, which is well above this minimum threshold for sustaining the oscillation.

Sustaining amplifier open loop measurement result. An open loop measurement setup is used to obtain the DC bias point and current consumption from a 1.8V source for the designed amplifier. The area consumption of the complete oscillator architecture in the absence of the bond pads is 0.121mm², as illustrated in Fig 9.

To obtain the forward transmission response of this sustaining amplifier, a -30dB_m of input power is applied to the RF_{in} port, to avoid saturation and the response is measured at RF_{out} with a 50Ω load termination.

In regards to the 17.22MHz operational frequency, the measured scattering parameter responses are plotted in Fig 10 for frequency measurement in a sweep between 1MHz to 50MHz and with a IF bandwidth of 100Hz. As observed in Fig 10, a maximum gain of 21dB is

Fig 6. Simulation model of resonator. a) Electrical lumped parameter of RLC model b) S_{21} simulated response of lumped parameter model.

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Table 1. Mechanical and Electrical Parameters for the C-C Beam Resonator.

	Parameter	Unit	Value
Mechanical Data	Effective stiffness, k	N/m	897
	Effective mass, m_{eff}	Kg	76 f
	Unloaded quality factor, Q	~~~~	1000
	Transduction gap	m	90n
Extracted and Measured Data	Electromechanical coefficient, k_{eff}^2	%	0.461
	Series resonance frequency, $f_s @ 5V_{DC}$	Hz	17.2631 M
	Parallel resonance frequency, $f_p @ 5V_{DC}$	Hz	17.30294 M
	Operating frequency, $f @ 5V_{DC}$	Hz	17.22 M
	Electromechanical coupling factor, η	C/m	85 n
Curve Fitted Electrical Data	Motional resistance, R_x	Ω	698 k
	Motional capacitance, C_x	F	8 a
	Motional inductance, L_x	H	10.6
	Feed-through capacitance, C_p	F	5.8 f
	Insertion loss	dB	76
	Transmission phase	$^\circ$	95

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achieved at 21MHz with a -3dB bandwidth of 40MHz which encapsulates the resonant frequency of the MEMS resonator. At the resonant frequency of 17.22MHz, the S_{21} magnitude is found as 19.48dB with a phase deviation of 12° . Hence, the loaded open loop gain at the resonant frequency, which is greater than 0dB ensures a sustained oscillation in closed loop configuration. This is also accompanied by the low phase shift of 12° at the resonant frequency which adequately satisfies the Barkhausen criteria.

Fig 7. Open loop responses of sustaining amplifier. a) Gain plot of 1st stage, 2nd stage, 3rd stage and complete amplifier b) Phase plots of 1st stage, 2nd stage, 3rd stage and complete amplifier.

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Table 2. Open Loop Gain and Phases of the Different Stages Amplifier.

Amplifier stage	1 st stage: Transimpedance Amplifier	2 nd stage: Intr. Voltage Amplifier	3 rd stage: Cascode Amplifier	Complete Amplifier
Gain	72 dBΩ	24 dB	30 dB	122 dBΩ
Phase (x°)	182	5	-255	-70

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MEMS-oscillator close loop response and figure of merit

In the close loop operation, the sustaining amplifier would provide the designed amount of gain to replenish all the motional losses. The unloaded quality factor of the MEMS device is only 1000 which is low enough to be competitive with the quartz counterpart and hence the phase noise measurement is crucial in its adaptation for an end-user specific application. In [Fig 11](#), the phase noise spectrum is shown at reference points of the complete circuit architecture with the settling time of 450μs and a voltage swing of 320mV for transient response in the post

Fig 8. Loop gain and phase response for the complete oscillator.

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Fig 9. Complete layout of the quartz oscillator with the integrated MEMS resonator.

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layout simulation, the close to carrier phase noise is given in Fig 11(b) and observed to be 83.898dBc/Hz at 1kHz offset, whereas the far out level is 103.76dBc/Hz at 10MHz offset (Table 3). To guarantee the robustness of the proposed architecture, phase noise performance across different extreme corners and temperature is tabulated, as shown in Table 3.

Fig 10. Measured forward transmission response of the sustaining amplifier chip. a) S_{21} gain plot b) S_{21} phase plot.

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Fig 11. Post layout simulated close loop responses of the oscillator. a) Transient response at the measurement port (Inset is the magnified stable part of the oscillation) b) Phase noises at different points of sustaining amplifier.

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The $1/f^3$ noise component, which dominates at 100Hz of offset frequency, consists of inter-modulation in carrier noise and transistor noise component. In a low quality MEMS, the capacitive nonlinearity is the apparent contributor towards the flicker frequencies [26].

The phase noise expression in Eq (16), describes the dependency among the various parameters.

$$L\{f_m\} \approx \frac{kTF}{2V_o^2} \left[\frac{R_x}{Q_l^2} \right] \times \left[\frac{C_x}{C} \right]^2 \times \left[\frac{f_0}{f_m} \right]^2 \quad (16)$$

Here, f_m is the offset from the carrier frequency at which point phase noise is being evaluated, V_o is the oscillator output voltage magnitude, $C = C_l$ is the external resonating capacitance, k is the Boltzmann's constant, Q_l is the loaded quality factor of the tank, and F is the

Table 3. Phase Noise at Different extreme corners in Post Layout Simulation.

PN Point, dBc/Hz		@ 1kHz	@ 10kHz	@ 100kHz	@ 1MHz	@ 10MHz
Process	Temperature (°C)					
All Typical	27 (reference)	-83.9	-101.22	- 97.58	- 100.1	-103.76
	-25	-85.27	-102.13	-98.41	-101.14	-104.59
	125	-82.51	-99.92	-95.98	-98.84	-102.4
All slow	-25	-83.44	-100.17	-96.02	-100.3	-102.8
	125	-81.39	-98	-93.6	-97.91	-100.2
All Fast	-25	-86.01	-102.2	-98.8	-102.7	-104.98
	125	-83.93	-100.36	-96.02	-100.3	-102.7

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noise figure of the sustaining amplifier. A much closer inspection, reveals the post layout simulated phase noise response of the curve in Fig 11 is found to have a slope of $1/f^3$ at low frequency offsets. This can be predicted by inspecting Eq (16) thoroughly or by realizing the scaling-induced noise theories. With respect to the stability of this oscillator, phase noise of -83.898dBc/Hz at 1kHz offset from the carrier is a limiting factor, which may have been contributed by the following causes.

- Non-linearity in the resonator capacitive transducer aliases $1/f$, electronic noise (e.g., from the sustaining amplifier) onto the carrier frequency, generating a $1/f^3$ component.
- $1/f$ noise associated with the DC polarization voltage on the resonator structure, which modulates the electrical stiffness k of the resonator [26, 27], inducing a $1/f^3$ phase noise component.
- $1/f$ mechanical noise which induces variations in the electrode-to-resonator gap spacing, which then modulates the electrical stiffness k , generating a $1/f^3$ phase noise component.

In reference to the oscillator application with the targeted Si micro-resonator, long term stability in material surface and noise performance are of significant concern among the above mentioned points where the limitation of non-linearity is the most likely mechanism, suspected to contribute towards additional noise being accounted in the phase noise spectrum [28] in achieving selectivity and sensitivity [26, 27]. The designed oscillator consumes 6.24mW of DC power, in the absence of the 50Ω buffer amplifier which was deliberately integrated for measurement purpose. In any clock IC application, there are other blocks, like fractional PLL, counter, etc. [29] for which the instrumentation buffer integration is alleviated.

In practical realization of the presented work as a fixed frequency reference oscillator in clock IC application, a high percentage of frequency yield is targeted in statistical analysis. In Monte Carlo analysis regarding a random variation for process and mismatch, 95% frequency yield in 20 number of run has been achieved [Fig 12(a)]. It is observable that the mean is closer to the desired frequency of oscillation of 17.22MHz , which is supported by the tabulated data in Table 4.

In Table 4, it is also observed that, the pad capacitance and buffer amplifier have no any additional ‘parasitics’ adversely affecting the frequency of oscillation. However, in the phase

Fig 12. Monte Carlo post layout simulation results. a) Histogram plot for ‘Yield of Frequency’ at 50Ω output port b) phase noise at 50Ω output port for different run.

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Table 4. Monte Carlo Results for Oscillation Frequency at Different Nodes.

Node Name	Mean	Standard Deviation
Cascade_stage_output	17.1950 MHz	8.44546 k
Buffer_amp_output	17.1950 MHz	8.44546 k
50 Ω port_output	17.195 MHz	8.445 k

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noise response seen in Fig 13, improvement in the 50 Ω measurement port is observed, as the buffer has added some additional gain without contributing into the noise power.

For the phase noise spectrum shown in Fig 12(b), noise floor converges at -104dB_c/Hz in all the run of the MonteCarlo, but as seen in Fig 13, the amplitude slightly varies, which seems to be the resultant of TIA generated noise and its effect on the overall bandwidth of interest. The gain can be made more stable by extending the bandwidth a bit further which may improve the amplitude fluctuation seen in Fig 13, where in additional, an automatic gain control (AGC) can reflect this benefit as well. Now, the integration of AGC is avoided in this work in exploiting the merits in simplicity of design and less power consumption. In reference to the low unloaded Q of 1000 of the Si-MEMS, the achieved phase noise is acceptable for the synthesized oscillator targeted towards real time clock (RTC) application. Also, the intended MEMS architecture is a temperature uncompensated resonator which preserves a further improvement avenue for the oscillator response.

A Figure of Merit (FOM) is necessary to define all the degrading factors affecting the performance being computed. The defined FOM will be able to relate mechanical limitations with the electrical performance and the operating temperature, so that a competitive comparison can be tabulated among various Q based oscillator designs and it is given in Eq (17), developed on the basis of S. Seth *et al.* work on PLL [30].

$$F.O.M = \frac{1}{PN_{Floor}} \times \frac{kT}{P_{DC}} \times f_o^2 \times R_x^2 \quad (17)$$

Fig 13. Transient response at 50 Ω output port in Monte Carlo simulation.

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Table 5. Design Parameters and Performance Comparison.

Parameter	Unit	[24]*†	[4]*†	[29]†	[14]†	[31]†	This work*†
MEMS Resonator							
Beam type	---	BAW	Tuning fork	T-shape	Nano-Plate	FBAR	Clamp-Clamp
Transduction Mode	---	Electrostatic	Electrostatic	Electrostatic	Electrostatic	Lateral field	Electrostatic
Frequency	Hz	35.3 M	1.2 M	1 M	167.8 M	1.17 G	17.22 M
Motional Resistance	Ω	1.36k	700k	200	145	135	698k
Quality Factor	----	1,800	3,029	20,000	1,084	2,200	1,000
Material	----	AlN on Si	AlCu on Si	AlN on Si	AlN/FeGaB	AlN on Si	Si
Sustaining Amplifier							
Process	m	500 n	350 n	180 n	500 n	500 n	180 n
Supply Voltage	V	3	2.5	1	2.2	-----	1.8
Transimpedance gain	dB Ω	83	126	-----	-----	-----	122
Configuration	---	Single	Single	Single	Single	Single	Single ended
Power consumption	W	3.8m	1.3m	3.2 μ	3m	3.5m	6.24m (including buffer)
Layout area	mm ²	1.96	0.052	0.1125	-----	-----	0.121
Oscillator							
Type	----	Monolith-ic	Monolith-ic	Monolith-ic	Wire bond	Monolith-ic	Monolith-ic
PN@1kHz	dBc/Hz	-108 (in HF mode)	-112	-70	-81.73	-81	-84
PN@10kHz	"	-130	-----	-85	-110	-112	-97
Noise Floor	"	-140	-120	-110	-130	-146	-102
F.O.M	Hz ² Ω^2	18.13	18.72k	0.47	6.224	202.12	0.94M

* Post Simulation results.

† Measurement results.

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Here, k is the Boltzman constant in J/kelvin, T is the temperature in kelvin, P_{DC} is the DC power consumption in watt, f_o is the operating frequency, PN is the phase noise floor and R_x is the motional resistance in Ω . In Table 5, the required comparison is shown where the FOM of this work has been found in an appreciating position as high as 0.94 Million, despite of its low Q , temperature uncompensated resonator or its lower range of operating frequency. As observed along with its possible monolithic integration, the reported MEMS oscillator can be adopted for a real time clocking IC application on the basis of the competitive results in Table 5.

The compared works used AlN compounds in resonator part, resulting in better power handling capability through thermal compensation [31], [32]. Such advantage is absent in the proposed architecture, yet achieving the highest FOM. The mechanical Q of the used Si resonator is much lower than the Q of other compared works. This is reflected in higher motional losses, but the proposed sustained amplifier design has fully compensated the bigger losses. Operating frequency can be seen higher in [24], [29], [14] than the reported work of 17.22 MHz and still the design has achieved a comparable phase noise values. So, the current design is delivering a high FOM for the comparatively lower cost MEMS resonator in similarly categorized crystal oscillator application. This ensures a possible 'low cost-high reliability' penetration in the miniaturized clock IC markets for the realized design. Additionally, this work has used 180nm process technology compared to 500nm of [14], [24], [31], which means, this design has to suffer from higher leakage current originated problems, like higher static power consumption, random fluctuations, worse gradients, increased diffusion effects, etc. But, the higher FOM of the present work has overcome many of these problems and ensured a small form factor of the

solution as well. Owing to the output buffer, the DC power consumption becomes relatively high. However, in practical applications, the buffer is not necessary.

Conclusion

A monolithically implementable Si-CMOS reference oscillator has been reported in this work. A 17.22MHz series resonant C-C beam Si-MEMS device which is used as a resonator along with a sustaining amplifier and an output buffer has been designed in the 180nm CMOS process. The sustaining amplifier is designed to compensate the MEMS motional losses with its 122dB Ω gain and designated phase shift. Open loop simulation supports the performance of the sustaining amplifier where measureable results have defended it. In close loop, the CMOS circuitry is optimized in this oscillator for a phase noise performance of -84dBc/Hz at 1kHz of offset as required for an application in clock generator IC. The MEMS resonator operates in flexural mode of vibration to produce the capacitive current and hence has very limited quality factor, observed as low as 1000. The small form factor and comparable phase noise with a very high figure of merit has made the solution feasible for monolithic fabrication. Moreover, 95% yield in desired operative frequency of oscillation in Monte Carlo simulation response has defended the possible integration of the design in Si-CMOS process for a clock IC application.

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Author Contributions

Conceived and designed the experiments: SR. Performed the experiments: SR EMF. Analyzed the data: AWR CCL. Contributed reagents/materials/analysis tools: HR. Wrote the paper: SR HR AWR.

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