RESEARCH ARTICLE

# A Novel Low-Ringing Monocycle Picosecond Pulse Generator Based on Step Recovery Diode

**Jianming Zhou\*, Xiao Yang, Qiuyuan Lu, Fan Liu**

School of Information and Electronics, Beijing Institute of Technology, Beijing, 100081, China

\* zhoujm@bit.edu.cn

## Abstract

This paper presents a high-performance low-ringing ultra-wideband monocycle picosecond pulse generator, formed using a step recovery diode (SRD), simulated in ADS software and generated through experimentation. The pulse generator comprises three parts, a step recovery diode, a field-effect transistor and a Schottky diode, used to eliminate the positive and negative ringing of pulse. Simulated results validate the design. Measured results indicate an output waveform of 1.88 peak-to-peak amplitude and 307ps pulse duration with a minimal ringing of -22.5 dB, providing good symmetry and low level of ringing. A high degree of coordination between the simulated and measured results is achieved.

## Introduction

Ultra-wideband narrow pulse is an important aspect of any study relating to ultra-wideband (UWB) radar and the UWB wireless communication system [1–3] owing to its high-resolution applications and simple system architecture. Numerous impulse radars have been developed for the purposes of detection, identification and scanning by analysis of transmitted and received signals [4–5]. The UWB narrow pulse can be further segregated into the classifications of step pulse, Gaussian pulse and the single-cycle pulse. All these pulses have wide frequency spectrums [6]. Step pulse and Gaussian pulse are suitable to be adopted to the receivers, because their high DC components are difficult to be emitted by the antenna. On the other hand, the single-cycle pulse can be used in the senders, owing to its lack of DC components and its minimal amount of low-frequency components.

In recent years, several studies have reported methods of generating UWB pulse, including the tunnel diode based generator [7], oscillator-based generator [8], transistor-based generator [9] and step recovery diode (SRD) based generators [1–2, 10–13]. Components should be carefully selected according to each system's unique requirements and depending on its output pulse power and width. The SRD-based is the most popular design method for all kinds of pulse generating solution, due to its effective ability to sharpen pulse transition edge [12] and its advantage of being easy to fabricate. However many researchers have encountered the same problem, namely, a high ringing level of the pulse, which has an undesirable effect on the resolution power

of sensing radars. In former research [14], we introduced a subnanosecond-wide Gaussian pulse using the shunt-connected SRD model, resulting in a ringing level of about -15dB. Through experimentation, [15] better results were attained, with a ringing level of -22dB, by using resistive stubs for suppressing the ringing tail. Nevertheless, the only shortcoming is that, the peak-to-peak pulse amplitude is very small (550mV) compared with other methods.

In this paper, our intention is to design a low-ringing monocycle picosecond pulse and to advance our former work [14, 16], with the aim of generating a signal which possesses both lower ringing and an acceptable amplitude. The remainder of this paper is structured as follows. Section II introduces the SRD model in brief. Section III describes the design circuit of the pulse generator. The test results achieved in the simulation and experiment are provided in Section IV, with conclusions provided in Section V.

## SRD Model

### 2.1 SRD structure and characteristics

SRD is a PN junction diode, whose impurity exhibits an unusual distribution, as shown in Fig 1. Between the high doping $P^+$ layer and the high doping $N^+$ layer is a low doping N-type layer. This has a typical slowly varying junction structure. The characteristics of forward conduction and reverse cut-off, produced by the excitement of a sine wave, will be presented to an ordinary diode. In the case of the SRD, the waveforms of current and voltage are different and are shown in Fig 2. When SRD converts from forward exciting voltage to negative exciting voltage, a strong backward current flows continuously until terminating at a time instant, thus forming a steep step voltage. The narrow pulse can be generated in this way.

The principles for this phenomenon are as follows:

1. When SRD is in a positive bias, both sides of the PN junction become infused with many minority carriers. The special impurity distribution in SRD facilitates the increase in these injected minority carriers, and creating retarding fields on both sides of the junction eliciting impedance in the minority carriers' proliferation, thus forming a concentration of minority carriers in the narrow regions near the junction. Furthermore, the increased
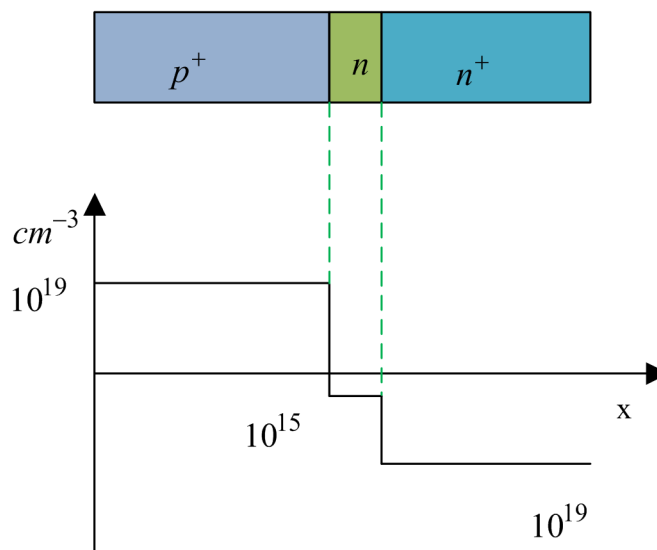


**Fig 1. Impurity profile of SRD.**

doi:10.1371/journal.pone.0136287.g001
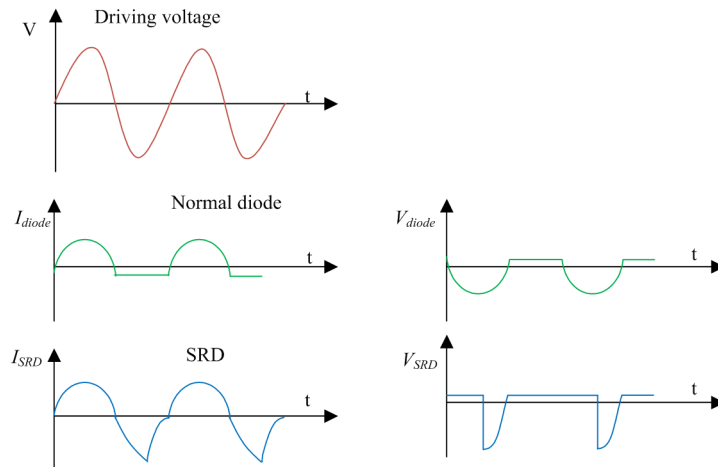
**Fig 2. Voltage and current characteristics curves of common diode and SRD.**

longevity of the minority carriers is such that they are prevented from rejoining during a period of positive bias.

2. When the positive bias converts to a negative bias, minority carriers stored will flow in the opposite direction to the injection, thus forming a strong backward current. When extraction of all the minority carriers has taken place, the backward current is suddenly reduced to an extremely low level, cutting off the diode and forming the step voltage.

## 2.2 SRD equivalent circuit analysis

The SRD equivalent circuit is depicted in Fig 3, where $C_f$ represents the forward-bias diffusion capacitance, $C_r$ denotes the backward-bias depletion layer capacitance, $R_f$ represents the junction resistance of the diode, $R_s$ denotes the series resistance of the diode, and $V_0$, the barrier potential of the junction. The equivalent circuit shows two types of working status in the forward and backward biases. Under the forward-bias voltage, the equivalent circuit consists of the large $C_f$ and $R_f$, whereas the equivalent circuit consists of the small $C_r$ under the backward-bias voltage.
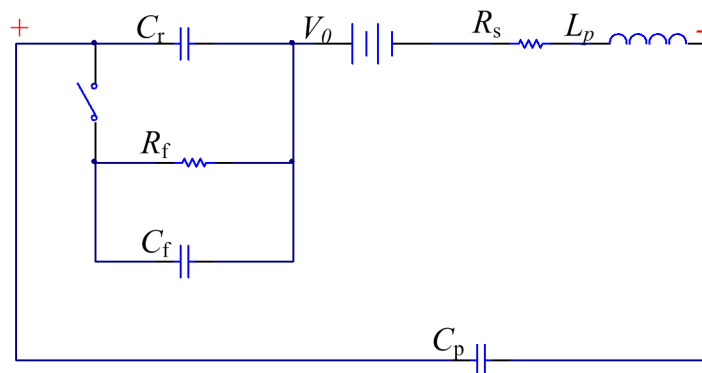


**Fig 3. Equivalent circuit of the SRD.**
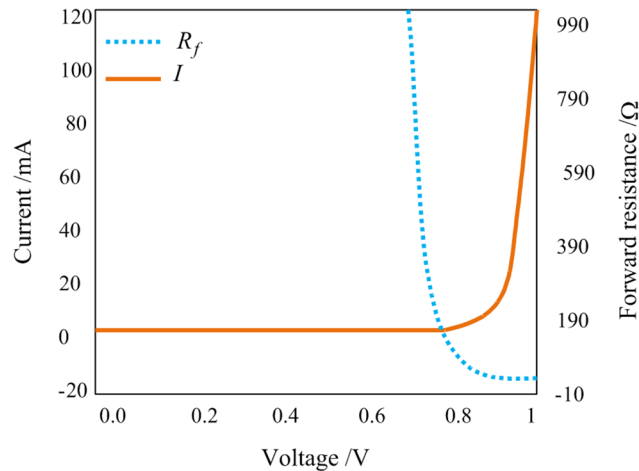
**Fig 4. *I-V* characteristic and forward resistance changing curves.**

Generally, the SRD parameters encompass $\gamma$, $C_0$, $V_0$ and $\tau$. According to Kotzebue's derivation:

$$\tau = R_f C_f \tag{1}$$

Where, $\tau$ is the lifetime of the minority carrier, and $C_f$ can be computed with $\tau$ and the forward on-resistance $R_f$. The forward resistance $R_f$ can be computed by measuring SRD's *I-V* characteristics. Typical *I-V* characteristics and forward resistance curves are shown in Fig 4. From the figure, it can be seen that the SRD's forward resistance $R_f$ is computed by measuring SRD's *I-V* characteristics, so the forward capacitance $C_f$ can be computed as well. With $\gamma$, $C_0$, $V_0$ and other diode parameters, the diode's model can be represented both easily and effectively. As the model is more accurate, consequent improvements to the hardware design are possible, along with speedier production rates in the design.

M-Pulse Microwave MP4023 is used as SRD in this paper. The parameters of $\tau$ is 15ns, $t_t$ (the transition time) is 50ps, $C_r$ is within 0.2~0.5pF, and $R_s$ is 0.8$\Omega$. The value of $C_f$ can be calculated by the existing parameters and the *I-V* curve, as show in Fig 4. When the values of all components in the SRD equivalent circuit are known, the Spice Model can be constructed according to the relationship between SRD quantity of electricity and voltage, as shown in Eq (2) [13].

$$Q(V) = \begin{cases} C_r V & V \leq 0 \\ \dfrac{C_f - C_r}{2V_0}\left(V + \dfrac{C_r V_0}{C_f - C_r}\right)^2 - \dfrac{C_r^2}{2(C_f - C_r)}V_0 & 0 < V < V_0 \\ C_f V - \dfrac{C_f - C_r}{2}V_0 & V \geq V_0 \end{cases} \tag{2}$$

Fig 5 presents the simulation diagram in ADS, where SDD denotes the relationship between current, voltage and their differentials of different ports in the N-port component. The component's properties can be expressed by defining the relationship between ports with their algebraic expressions. By representing the voltage-current relation in Eq (1) with SDD and defining the SRD parameters of $C_f$ and $C_r$ that have been acquired above as the input, we can obtain the simulation model.
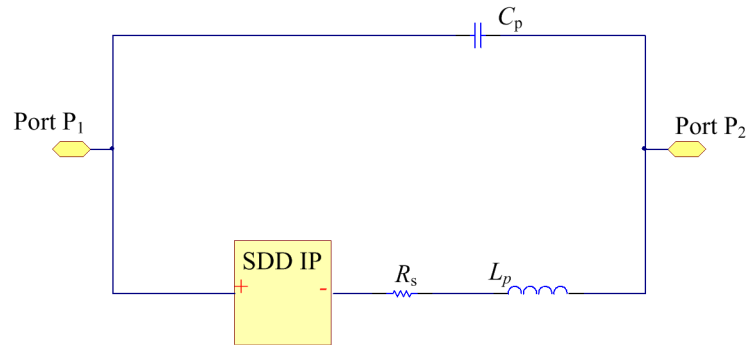
**Fig 5. Spice model of the SRD.**
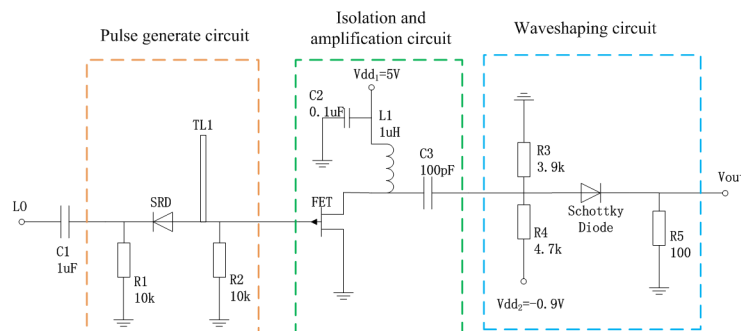
doi:10.1371/journal.pone.0136287.g005

## Pulse Generator Circuit Design

### 3.1 Overall design

To generate the required Gaussian narrow pulse, the circuit of the pulse generator is designed based on the prototype in [2], in which the small amplitude of output signal highlights an inevitable shortcoming. In order to overcome this issue, we add a FET module to amplify the output pulse signal. In addition, another function of the FET module is to act as a buffer between the signal generating module and the signal shaping module. Fig 6 shows the overall circuit design of the pulse generator, which consists of a pulse generating circuit, isolating and amplifying circuit, as well as the shaping circuit. The pulse generating circuit comprises a coupled circuit, match circuit, step recovery diode (SRD), and a micro-strip short-circuit line. The isolating and amplifying circuit consists of FET module, with the shaping circuit being made up of Schottky diode. A summary of parameters of main component in Fig 6 appears in Table 1, and other values for resistances and capacitances are marked in the figure.

### 3.2 Pulse generating circuit

The input periodic square wave signal excites SRD via the coupled circuit and the match circuit. The SRD self-bias circuit, consisting of the coupled circuit and $R_L$, eliminates the need for the extra DC biasing circuit, thereby reducing the overall size of the circuit, exercises good control over charge storage and ensures an optimum output of the pulse at high amplitude. The match circuit is used to achieve maximum transmission of power, owing to the input impedance of SRD being within the range 10–20Ω, while the input impedance of the entire system is



**Fig 6. Circuit of the picosecond pulse generator.**

doi:10.1371/journal.pone.0136287.g006

Table 1. Parameters of main components of circuit.

| Function | Type | Key parameter |
| --- | --- | --- |
| Signal input | Square wave | 10MHz |
| Substrate | FR-4 | $\varepsilon_r = 9.6$ |
| SRD | MP4023 | $\tau = 15ns$, $t_t = 50ps$, $C_r = 0.2\sim0.5$ pF |
| Transmission line | TL1 | 400 mil |
| Schottky diode | HSMS2820 | Turn-On Voltage 0.34 V at 1 mA |
| FET | FSX017LG | $I_{DSS} = 55mA$, $C_{GS} = 0.55pF$ |

doi:10.1371/journal.pone.0136287.t001

$50\Omega$. Furthermore, an extremely fast step pulse can be generated after the signal passes through SRD. In addition, it will yield a narrow pulse with a long tail and width by subtracting the forward-propagation step pulse from the reflected step pulse after passing through the micro-strip short-circuit line. Therefore the process needs to be carried out by the subsequent circuits.

The following matter requires special consideration during the design process. The length of the micro-strip short-circuit line is determined by the pulse width, as shown in Eq (3).

$$t_A = \frac{2l}{v} \tag{3}$$

Where, $t_A$ denotes the pulse width, $l$ represents the length of the micro-strip short-circuit line, and $v = \frac{c}{\sqrt{\varepsilon_{re}}}$ (c is the speed of light), $\varepsilon_{re}$ is effective dielectric constant. According to Eq (3), the length of the short-circuit line can be acquired after the pulse width $t_A$ is achieved.

## 3.3 Isolating and amplifying circuit

The function of FET module has two aspects, the first and more important role is to amplify the pulse signal, and the other is to isolate the pulse generating circuit from the pulse shaping circuit, which can be seen in the Fig 6. The working principle of the amplifier circuit is as follows: the positive DC bias voltage is applied to the drain electrode of FET by $V_{dd1}$, and the pulse signal generated by MP4023 is connect to the grid electrode. Before the narrow pulse coming, FET is functioning in a saturation zone and fails to work. However, when the negative pulse arriving, FET works in the linear amplification zone due to the negative bias voltage, and amplifies the narrow pulse signal. After being amplified by FET, the narrow pulse will be of larger amplitude and convert from a negative pulse to a positive pulse.

## 3.4 Function of Schottky Diode

The ringing level of pulse signal is further reduced by the Schottky diode in the shaping circuit, serving as a high-speed switch, which only allows a pulse greater than a certain threshold to pass. This threshold is determined by the DC bias voltage $V_d$. The negative bias voltage can lower the pulse form overall and theoretically eliminate any positive and negative ringing. Despite this, it is impossible as the switch time of the Schottky diode could not be equal to zero. So the phenomenon of ringing still exists in the output and the value of $V_d$ is determined by the value of the ringing. In this design, the $V_d$ is set by -0.9V, as shown in Fig 6.

## Simulation and Experimental Results

According to the SRD model and designed circuit as shown in Fig 6, we simulate the pulse generator in ADS software. Fig 7 shows the waveform of the output pulse in simulation. In the figure, the SRD model has been applied to the pulse generator. One can see that the pulse width is
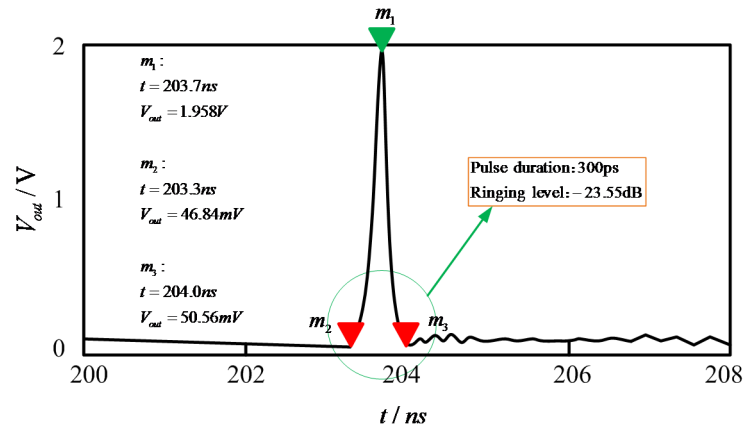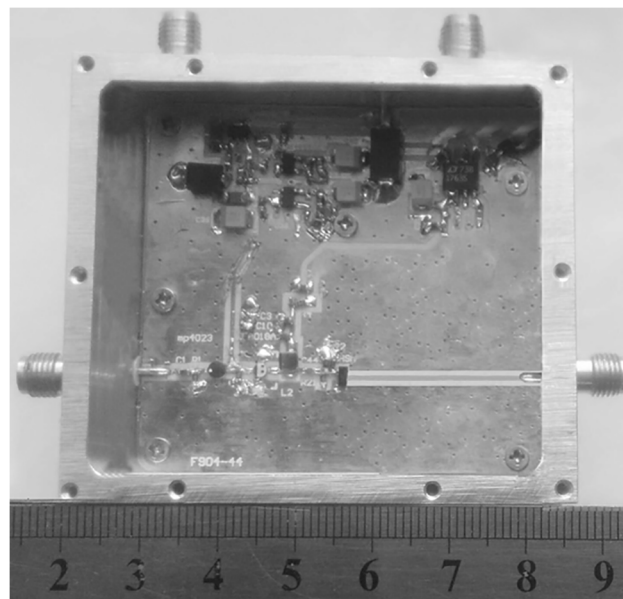
**Fig 7. Simulation of the output pulse.**

doi:10.1371/journal.pone.0136287.g007

about 300ps and the pulse amplitude is about 1.96 V. The waveform in the simulation is satisfactory because nearly all tails and ringing have been eliminated.

The detailed ringing level $R_l$, can be calculated by Eq ([4](#)), which was reduced to -23.55dB, with the peak-to-peak amplitude of ringing at about 130mV.

$$R_l = 20\log\frac{Amplitude\ of\ ringing_{peak-to-peak}}{Amplitude\ of\ pulse_{peak-to-peak}} \tag{4}$$

The circuit of the pulse generator is made utilizing Teflon boards. Its permittivity is 9.6, its density 0.8mm, and the micro-strip line is 50Ω. The design of the circuit structure is compact, as shown in [Fig 8](#). The input signal is 10 MHz rectangular wave, and the waveform is monitored by Lecroy Wave Master 8600A 6GHz DSO oscilloscope as shown in [Fig 9](#). The pulse amplitude is 1.88 V and the pulse width is 307ps. A comparison between the experimental



**Fig 8. Prototype of designed pulse generator.**

doi:10.1371/journal.pone.0136287.g008
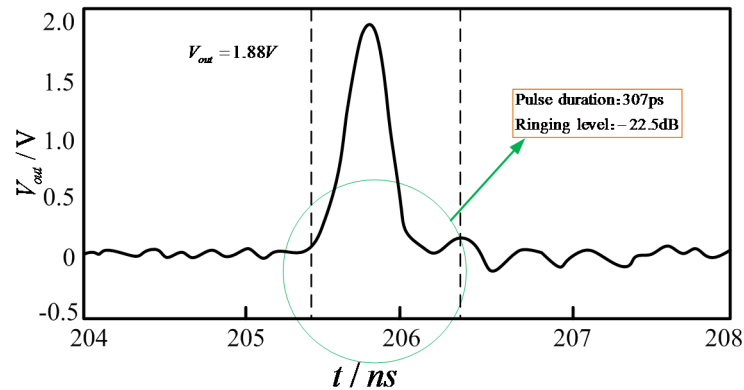
**Fig 9. Measured output pulse of the generator.**

result and the simulation result demonstrates that the pulse amplitude in the test is smaller than that in the simulation, and the pulse ringing in the test is greater than that in the simulation. The ringing level of pulse is -22.5dB, with the peak-to-peak amplitude of ringing being 135mV. Overall the two basic results are consistent. Moreover, the generated narrow pulse is highly symmetric and without huge tails and ringing.

Furthermore, in order to evaluate the performance of the proposed pulse generator, a comparison of various UWB pulse generators constructed from discrete components which have been used in recent research has been given as shown in Table 2. It can be inferred that our design has a very low ringing level [2, 10, 12, 13] and narrow pulse [10, 12, 13]. In [2], the circuit was more complicated and exhibited an increase in power consumption owing to the second DC bias Schottky Diode. It can be said however, compared to the literature noted in [12, 14], which also possess relatively low ringing results, that our designed pulse achieves an acceptable amplitude.

## Conclusion

A SRD model is constructed by using ADS simulation software in this paper. The researchers also design, simulate, construct and test a UWB picosecond pulse generator. The proposed generator proves to be structurally compact, cheap to build and easy to implement. The width and amplitude of the tested pulse are 307ps and 1.88V respectively. The test results are consistent with the simulation results. The proposed generator can therefore be adapted to practical

**Table 2. Comparisons with pulse generations in literatures.**

| Reference | Pulse amplitude /V | Pulse duration /ps | $R_l$ /dB |
|---|---|---|---|
| [1] | 0.7 | 350 | -20.9 |
| [2] | 0.4 | 300 | -17 |
| [10] | 0.2 | 600~780 | -20 |
| [12] | 0.87 | 170 | -22 |
| [13] | 1.8~1.85 | 1000 | -17.15 |
| [14] | 15 | 400 | -15.56 |
| [15] | 0.55 | 320 | -22 |
| This work-S | 1.96 | 300 | -23.55 |
| This work-E | 1.88 | 307 | -22.5 |

applications and be introduced to either UWB pulse emitting components or down-conversion sampling receivers. We conclude that this model has great potential to be widely used.

## Author Contributions

Conceived and designed the experiments: JZ XY FL. Performed the experiments: QL FL. Analyzed the data: JZ XY QL. Contributed reagents/materials/analysis tools: JZ. Wrote the paper: JZ XY.

## References

1. Lee JS, Nguyen C, Scullion T (2001) New uniplanar sub-nanosecond monocycle pulse generator and transformer for time-domain microwave applications. IEEE Transactions on Microwave Theory and Techniques 49: 1126–1129. doi: 10.1109/22.925501

2. Han J, Nguyen C (2002) A new ultra-wideband, ultra-short monocycle pulse generator with reduced ringing. IEEE Microwave Wireless Components Letters 2: 206–208. doi: 10.1109/LMWC.2002.1009996

3. Han J, Nguyen C (2006) on the development of a compact sub-nanosecond tunable monocycle pulse transmitter for UWB applications. IEEE Transactions on Microwave Theory and Techniques 54: 285–293. doi: 10.1109/TMTT.2005.860299

4. Benedetto F, Benedetto MR, De Blasiis MR, Giunta G, (2005) Reliability of signal processing technique for pavement damages detection and classification using ground penetrating radar. IEEE Sensors Journal, 5: 471–480. doi: 10.1109/JSEN.2005.846176

5. De Angelis A, Dionigi M, Moscitta A, Carbone P, (2009) A low-cost ultra-wideband indoor ranging system, IEEE Transactions on Instrumentation and Measurement. 58: 3935–3942. doi: 10.1109/TIM.2009.2020834

6. Andrews JR, (2003) UWB signal sources, antennas and propagation, IEEE Topical Conference on Wireless Communication Technology. 15–17: 439–440. doi: 10.1109/WCT.2003.1321594

7. Ruai YY, Konishi Y, Allen ST, Reddy M, Mark JW, (1994) A traveling-wave resonant tunnel diode pulse generator, IEEE Microwave and Guided Wave Letters. 4: 220–222. doi: 10.1109/75.298246

8. Teshirogi T, Saito S, Uchino M, Ejima M, Hamaguchi K, Ogawa H, Kohno R, (2005) Residual-carrier-free burst oscillator for automotive UWB radar applications, Electronics Letters. 41: 535–536. doi: 10.1049/el:20050604

9. Gerding M, Musch T, Schiek B, (2004) Generation of short electrical pulses based on bipolar transistors, Advances in Radio Science. 2: 7–12. doi: 10.5194/ars-2-7-2004

10. Han J, Nguyen C, (2005) Coupled-slotline-hybrid sampling mixer integrated with step-recovery-diode pulse generator for UWB applications, IEEE Transactions on Microwave Theory and Techniques. 53: 1875–1882. doi: 10.1109/TMTT.2005.848091

11. Protiva P, Mrkvica J, Machac J, (2010) A Compact Step Recovery Diode Subnanosecond Pulse Gnerator, Microwave and Optical Technology Letters. 52: 438–440. doi: 10.1002/mop.24945

12. Kamal1 A, Bhattacharya A, Tamrakar M, Roy C, (2014) Low-ringing and reduced-cost step recovery diode based UWB pulse generators for GPR applications, Microwave and Optical Technology Letters. 56:2289–2294. doi: 10.1002/mop.28581

13. Xia T, Venkatachalam AS, Dryver H, (2012) A high-performance low-ringing ultrawideband monocycle pulse generator, IEEE Transactions on Instrumentation and Measurement. 61: 261–266. doi: 10.1109/TIM.2011.2161022

14. Zhou JM, Gao XW, Fei YC, (2006) A new CAD model of step recovery diode and generation of UWB signals, IEICE Electronics Express. 3: 534–539. doi.org/10.1587/elex.3.534

15. Ma TG, Wu CJ, Cheng PK, Chou CF, (2007) Ultrawideband monocycle pulse generator with dual resistive loaded shunt stubs, Microwave and Optical Technology Letters. 49: 459–462. doi: 10.1002/mop.22145

16. Liu BS, Zhou JM, Zhou J, (2012) An improved ultra-wideband, ultra-short monocycle pulse generator, Advanced Materials Research. 588–589: 781–784. doi: 10.4028/www.scientific.net/AMR.588-589.781